Picometer-Resolution MEMS Segmented Deformable Mirror

NASA Phase I SBIR: NNX11CE94P

Dielectric Coating of MEMS Deformable Mirrors

NSF Phase I SBIR: IIP-1014435

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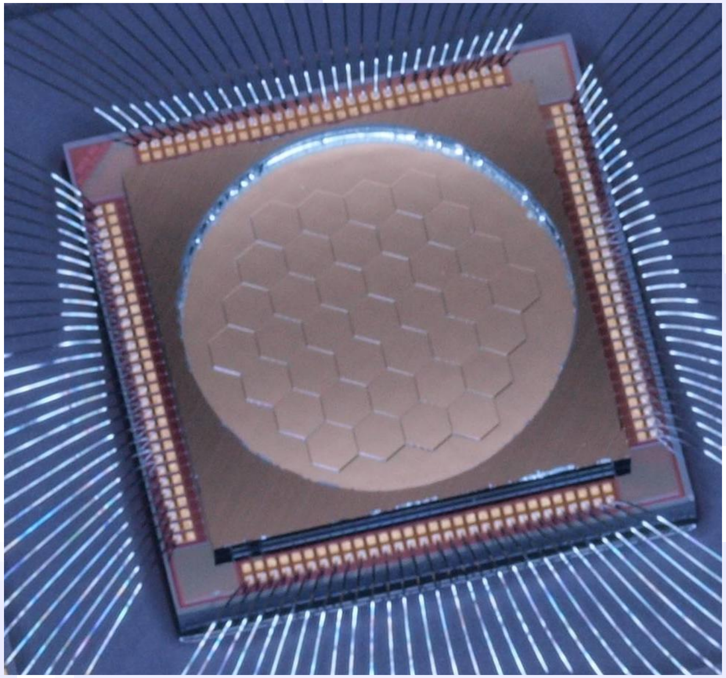
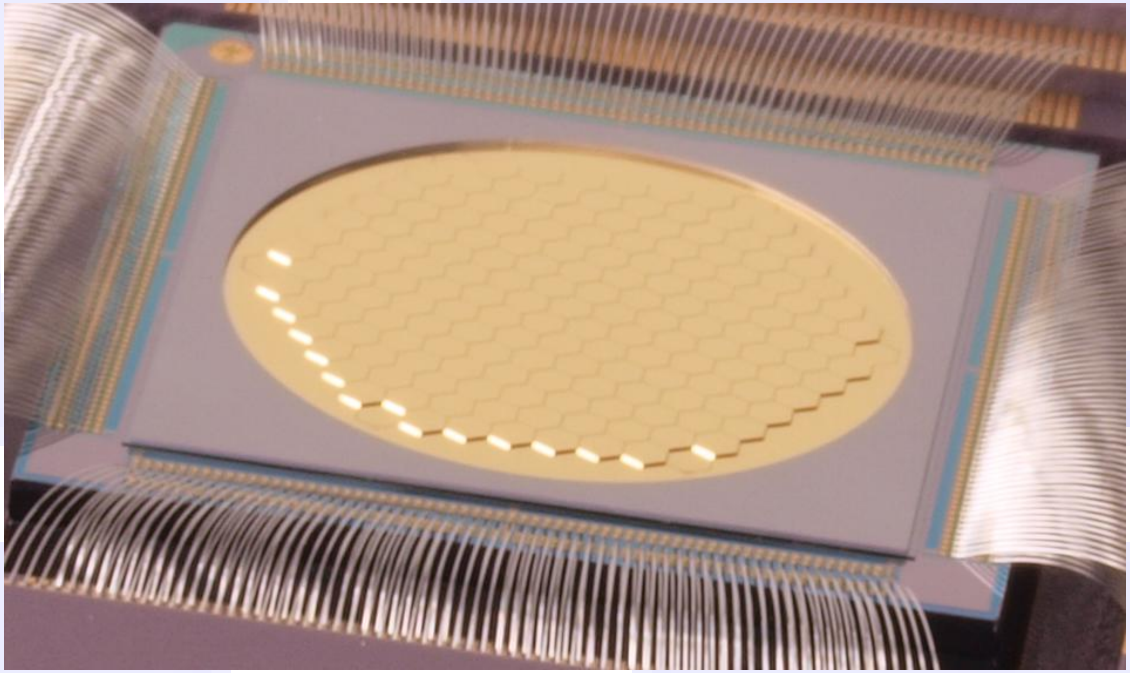
Iris AO MEMS Segmented Deformable Mirrors





PTT111 DM
- **111 Actuators**
- **37 PTT Segments**
- **3.5 mm inscribed aperture**
- **Factory calibrated**

PTT489 DM
- **489 Actuators**
- **163 PTT Segments**
- **7.7 mm inscribed aperture**
- **Factory calibrated**

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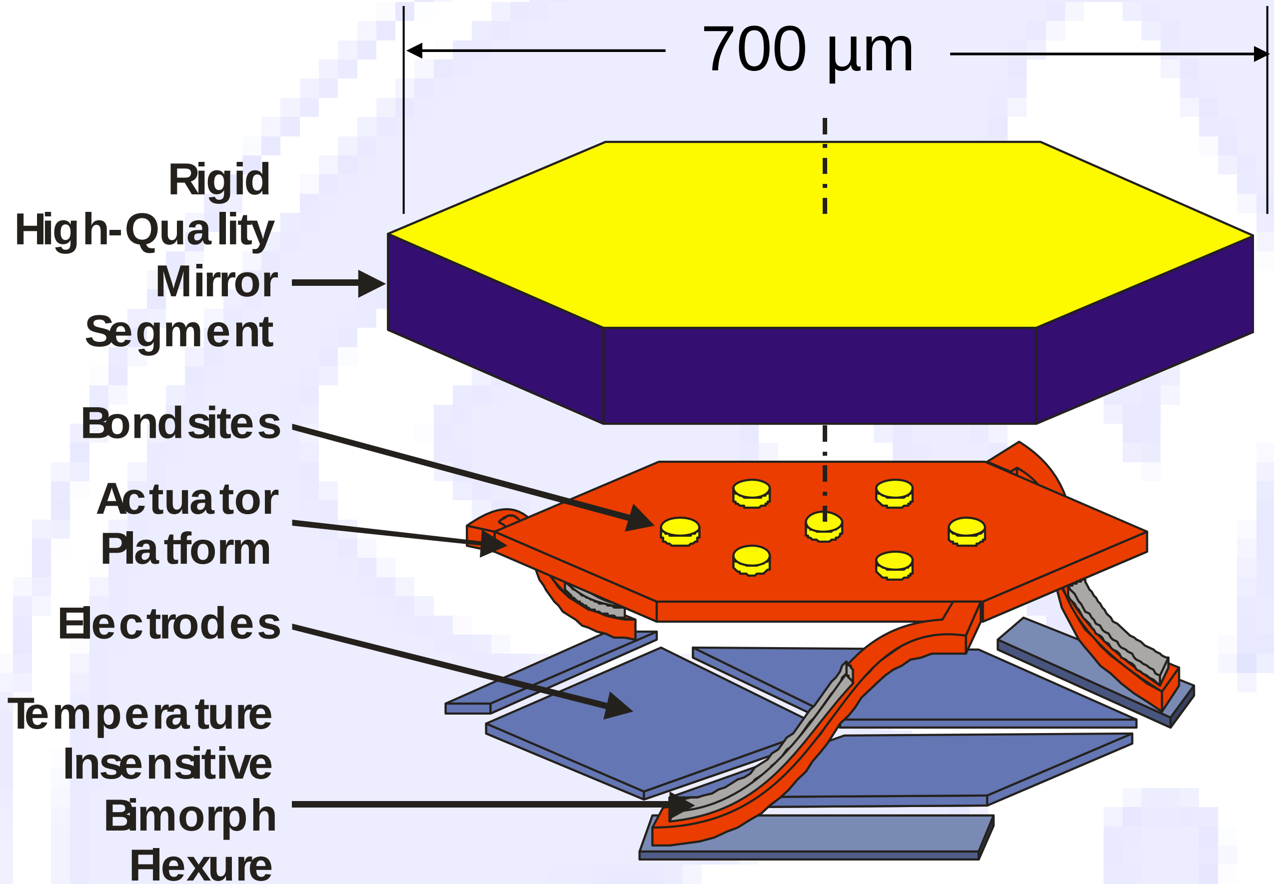
Iris AO Segmented DM Background



- 3 DOF: Piston/tip/tilt electrostatic actuation – no hysteresis
- Hybrid fabrication process
  - 3-poly surface micromachining
  - Single-crystal-silicon assembled mirror
- Unit cell easily tiled to create large arrays
- Hybrid technology
  - Thick mirror segments
  - Enables back-side stress-compensation coatings

Small
Business
Innovation
Research

Picometer-Resolution MEMS Segmented DM – Phase I SBIR

Iris AO, Inc.
Berkeley, CA

INNOVATION

Design and fabrication process improvements to reduce unpowered surface-figure errors from MEMS-based deformable mirrors.

TRL Assessment - Start: 3/4 End: 3/4

TECHNICAL ACCOMPLISHMENTS

- Codified systematic and random effects that contribute to un-powered mirror segment position variations of 1st generation PTT489 DM prototypes
- Modified fabrication process to reduce low-order chip bow
- Preliminary development of post-processing technique to compensate for chip-bow variations
- Modified DM segment design to make it more robust to misalignment and manufacturing tolerances

FUTURE PLANS

- Implement design and fabrication process changes on a production run of the a 489 actuator 163-piston/tip/tilt-segment deformable mirror
- Build a 939-actuator, 313-PTT segment DM

GOVERNMENT/SCIENCE APPLICATIONS

- PTT489 DM being used for the Extrasolar Planetary Imaging Coronagraph (EPIC), PI: Mark Clampin, NASA/GSFC
- PTT111 DM (111-actuator, 37-piston/tip/tilt segment) used as a hardware simulator to test co-phasing of the JWST segments
- Extend to 1000 actuator devices for high turbulence imaging and laser communication applications (DoD) and 3000 actuators for high-contrast imaging applications (NASA)
- Demonstrate control to XX nm

PTT489-5 DM

COMMERCIALIZATION

- Commercially Available Products:
  - PTT111 and PTT489 deformable mirrors
  - Smart Driver II: High voltage drive electronics
  - PTT111 and PTT489 AO Engine: Closed-loop adaptive optics system
- 6 patents awarded
- DMs purchased by academic and commercial researchers in vision science, ophthalmology, laser manufacturing, astronomy, and defense
- Better SWAP compared to piezoelectric stacked-actuator DMs
- No hysteresis
- Factory calibrated position controller linearizes operation and limits operation to safe bounds.
- Larger stroke than competing large-actuator technologies while maintaining speed

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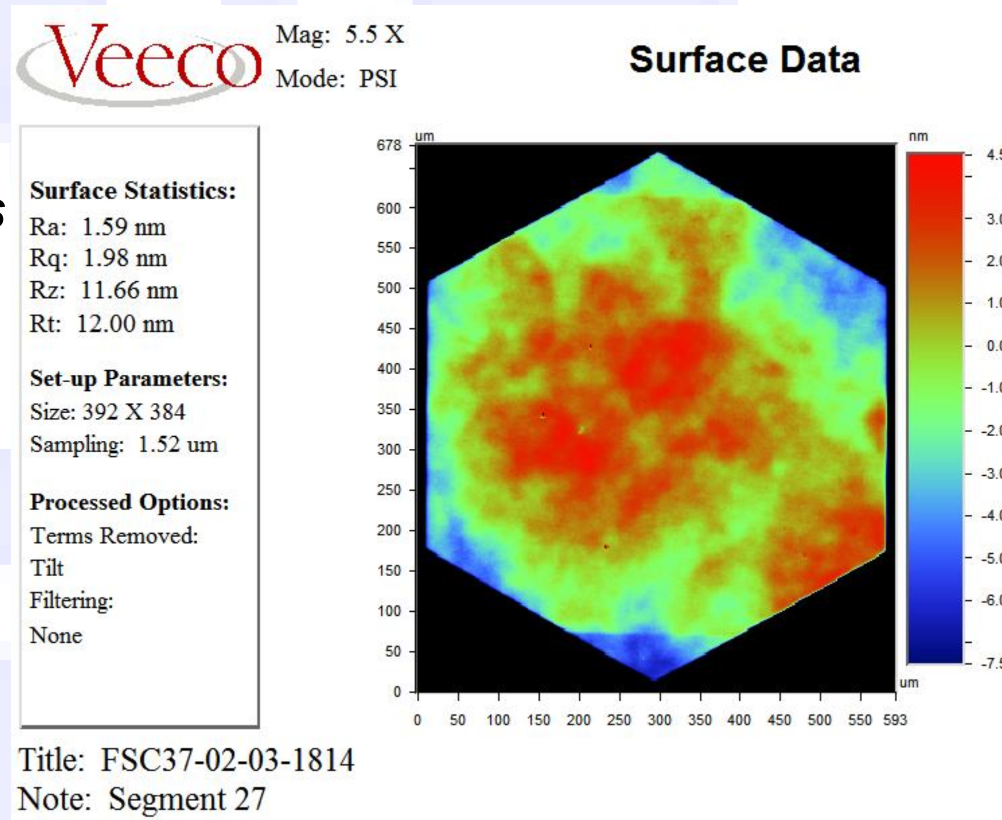
Exoplanet Imaging Requirements: *VNC Technology*

- **Usable Dynamic Range (Stroke): 0.5 µm**
- **Segment Control Resolution: 25 pm**
- **~1000 Segment DM**

- **Segment Flatness: 1-3 nm *rms***
  - **2 nm *rms* demonstrated**
- **Robust to snap-in failures**
  - **Anti-snap-in device (ASD) technology survives 100M snap-in events**



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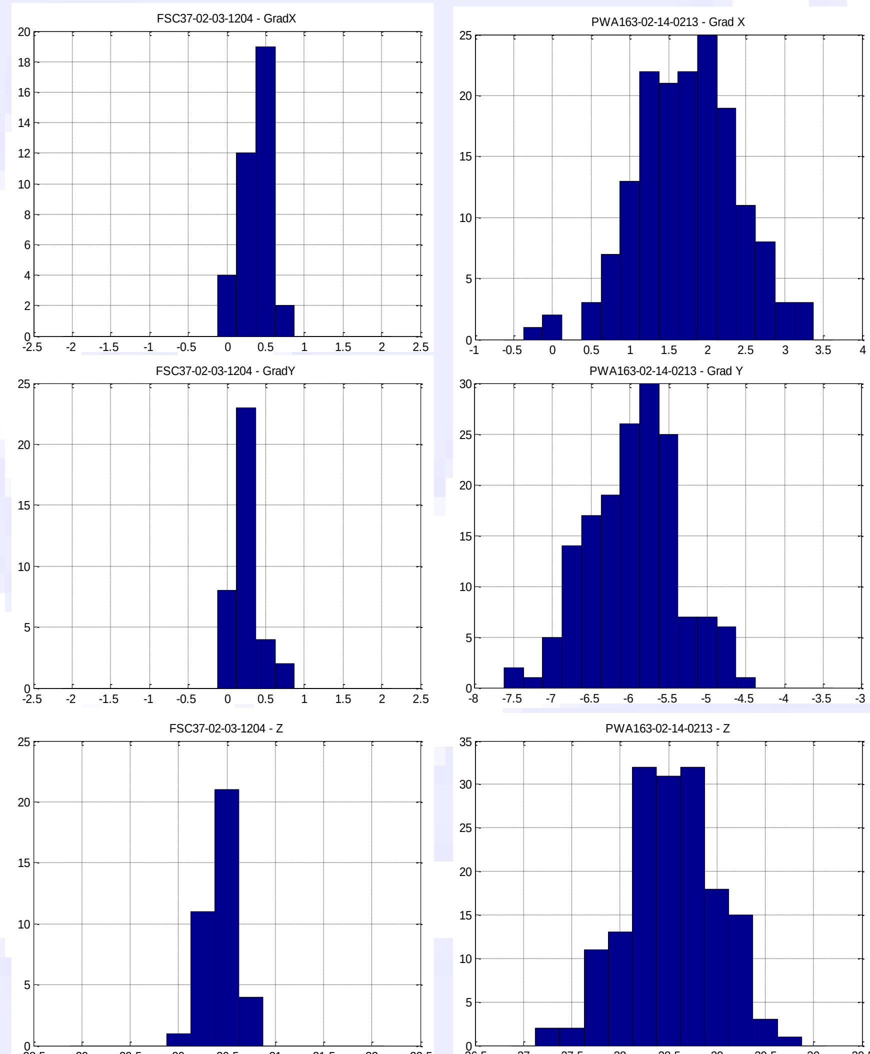
PTT489 DM Prototypes (First Silicon): *Pre-Phase I Background*

- **Best DM – 1 bad segment**
  - **> 5µm stroke**
    - **Too large for 25 pm resolution requirement**
  - **Mirror flatness: < 3 nm *rms* over 400 µm region**
- **Worst DMs: Excessive systematic segment tilts**
  - **Root cause – misaligmnent during contact photolithography**
- **Relatively large random segment positions**
  - **Larger variations in contact photolithography compared to stepper lithography**



PTT111 DM **PTT489 DM**

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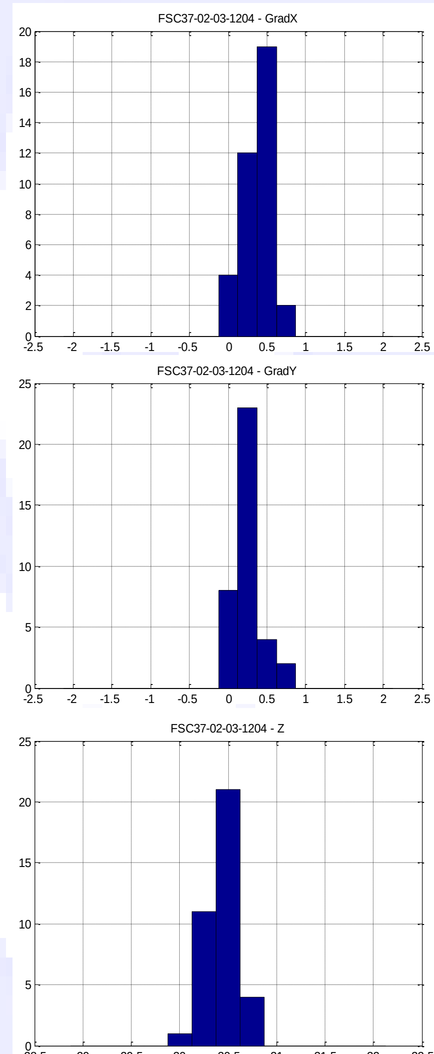
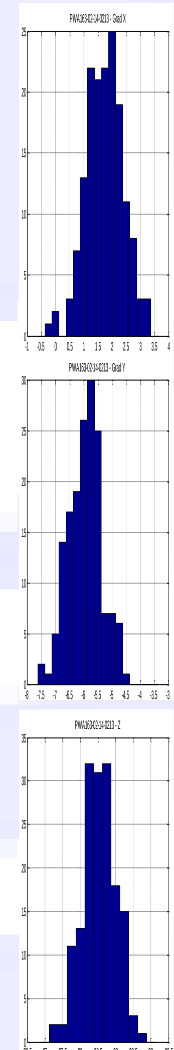
Phase I SBIR Goals

- **Mitigate unpowered segment-position variations that reduce usable range**
- **Floor-plan design of PTT939 DM**



PTT111 DM



PTT489 DM

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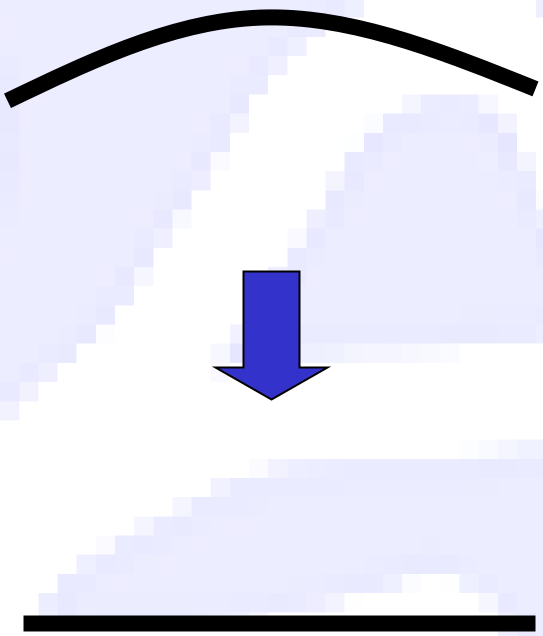
Phase I Development – Chip Bow

- Systematic: stresses in thin films on top of wafer
  - Layer thicknesses modified to reduce net bow
  - Modifications to be implemented in production run
- Random: run-to-run and wafer-to-wafer variations in thin-film stresses
  - Post-process compensation technique developed
  - Variation of curvatures should be covered



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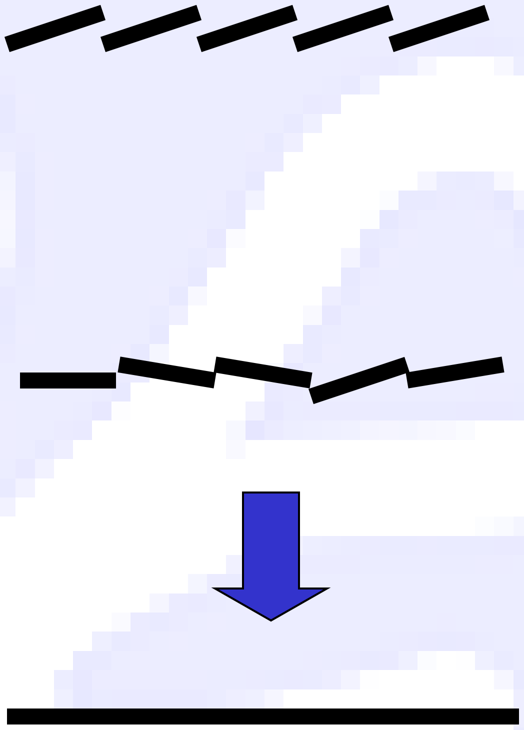
Phase I Development – Segment Position Variations

- Systematic tilts from misalignment during lithography
  - Designed self-aligned structures
- Random segment positions
  - Modified designs to make less susceptible to dimensional variations
- Short-loop run to demonstrate design modifications
- Will be implemented in production run
  - Incorporate ASD technology



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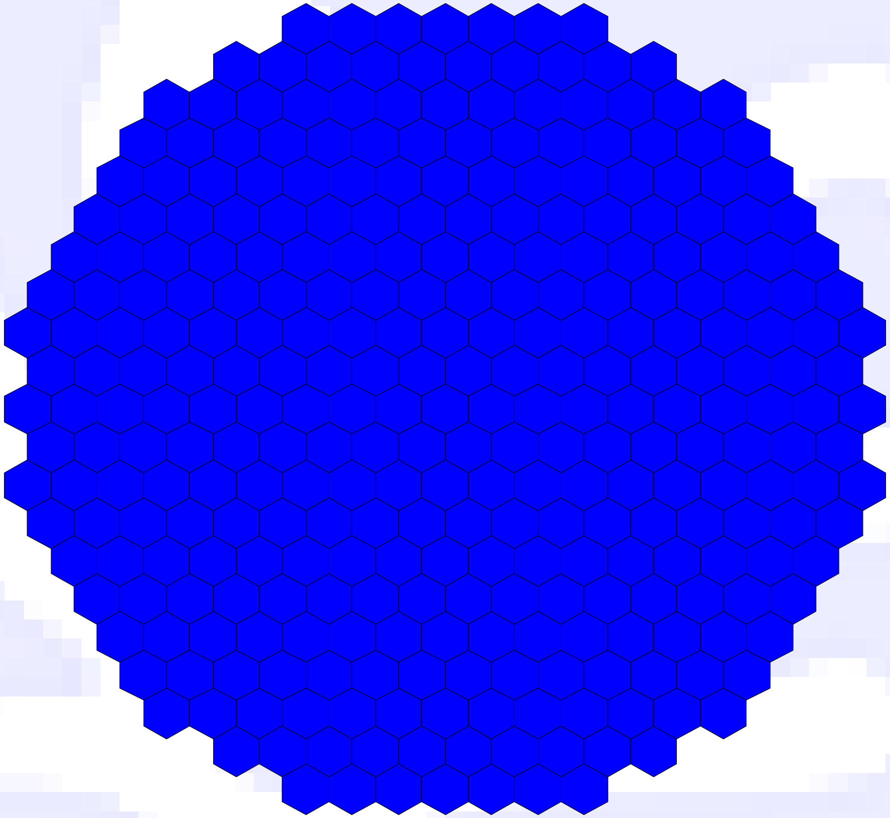
PTT939 Design: *Towards 1000 Segments*

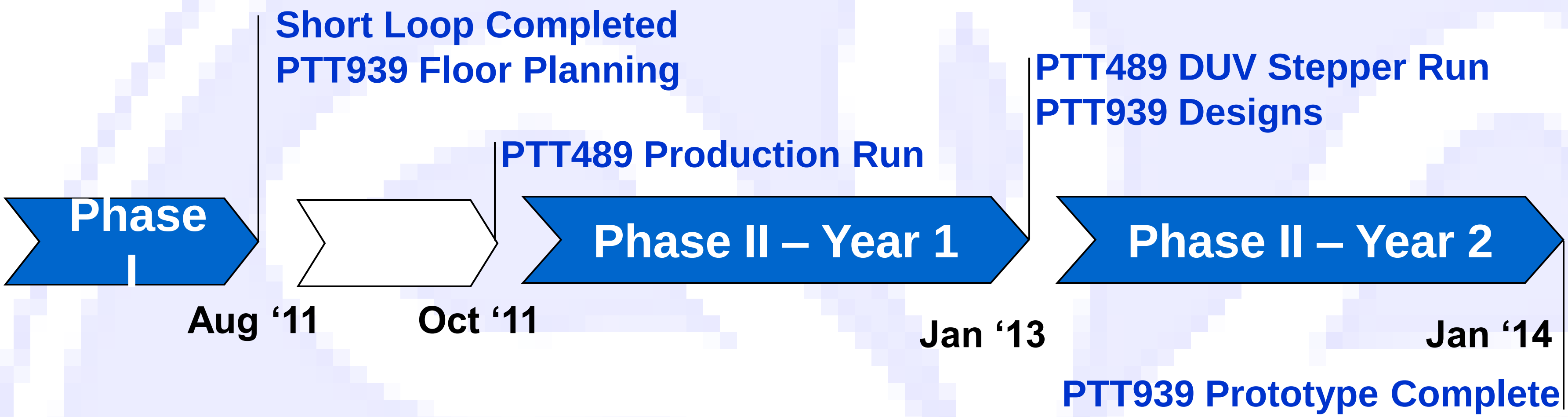
- **939 Actuators**
- **313 PTT Segments**
- **10.85 mm aperture**



Phase II Goals

- Improve unpowered segment position errors: < 200-300 nm *rms*
  - Analyze PTT489 production run results
  - Modify designs for lithography using DUV stepper
- Complete PTT939 design
- Fabricate PTT939 prototypes

Future Development Timeline



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Dielectric Coating of MEMS Deformable Mirrors

Iris AO, Inc.
Berkeley, CA

INNOVATION

Design and fabrication process developments to enable use of DMs with high-power lasers. Developments enable application of highly-reflective dielectric coatings onto DMs that range from 355 nm to 1540 nm.

TRL Assessment - Start: 2/3 End: 3/4

TECHNICAL ACCOMPLISHMENTS

- Developed a compensation layer to enable dielectric coating of DMs for 1064 and 1540 nm
- Fabricated mirror arrays with compensation coatings
- Demonstrated $\lambda/20$ coatings at 532nm, 1064nm and 1540 nm
- Conducted laser testing showing ability of DMs with existing packaging to handle 150 W/cm^2
- Laser testing and models show with heatsinking, 1200 W/cm^2

FUTURE PLANS

- Improve DM design to enable >2000 W/cm^2 power handling
  - Heatsinking
  - Compensate for CTE mismatches
  - Reduce segment gaps

GOVERNMENT/SCIENCE APPLICATIONS

- Laser guidestar uplink correction
- Free-space laser communications
- Potential DoD and Directed Energy Applications
  - Designator lasers
  - Probe beams for HEL systems
  - Countermeasures for heatseaking missiles
- Extend power handling to >2000 W/cm^2
- Increase DM size

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- High-speed focus correction and beam shaping for laser micromachining
- Better SWAP compared to piezoelectric stacked-actuator DMs
- No hysteresis
- Factory calibrated position controller linearizes operation and limits operation to safe bounds.
- Larger stroke than competing large-actuator technologies while maintaining speed

Approved for Public Release

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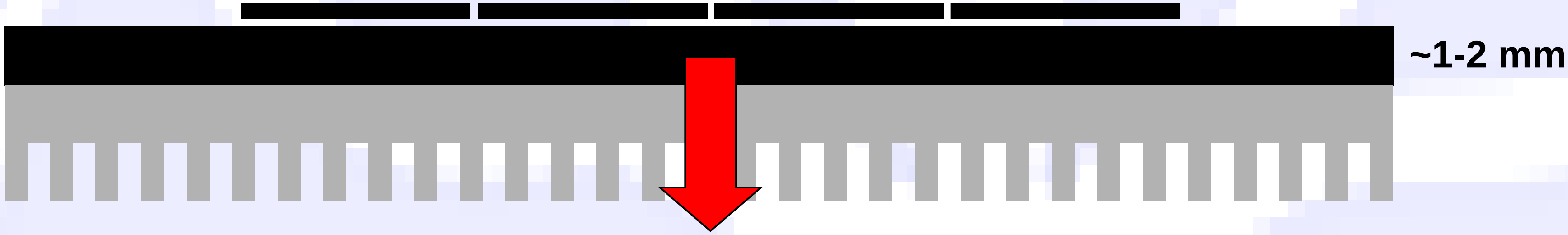
MEMS Benefit: *Short Thermal Paths*

- **MEMS are planar devices**
  - **Short thermal path to heatsinks possible**



Dielectric Coatings

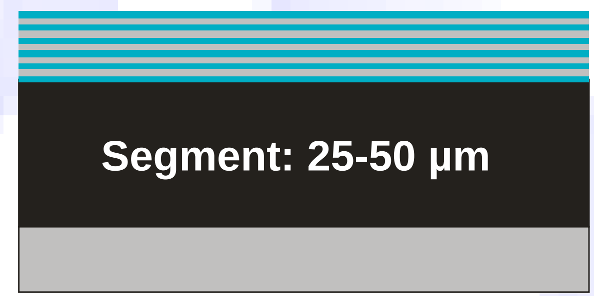
- **Damage thresholds: >100X of metal coatings**
- **Coating thickness: ~5x λ**
- **Coating temperature: 300-400 °C**
- **Residual stress**
  - **Up to 100 MPa**
  - **Can be humidity dependent**

- **Thicker Segments – 50 μm**
- **Stress compensation layer**

- **1st demonstration of customized DM for dielectrics**
  - **>99.9% reflectance dielectric coatings @ 532 nm**
  - **< 30 nm rms residual surface figure errors**
  - **~2.6 μm thick coating**
  - **PV deformation: ~1nm/°C**

Dielectric Coating

Dielectric Coating



Stress Compensation Coating

Phase I Goals

- Demonstrate stress-compensation for 1064 nm and 1540 nm coatings
  - Figure errors < $\lambda/20$
- Test laser-power-handling of 532 nm DM
- Develop thermal models

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Phase I Coatings: *1064 and 1540nm*

- Stress testing of 1064 and 1540 nm coatings
- Compensation layer design
- Mirror-wafer fabrication with compensation layer
- DM array fabrication and coating
- 1064 nm
  - >99.85%
  - Coating thickness: 5.4 µm
  - Segment figure errors: <λ/20
- 1540 nm
  - >99.85%
  - Coating thickness: 7.9 µm
  - Segment figure errors: <λ/20

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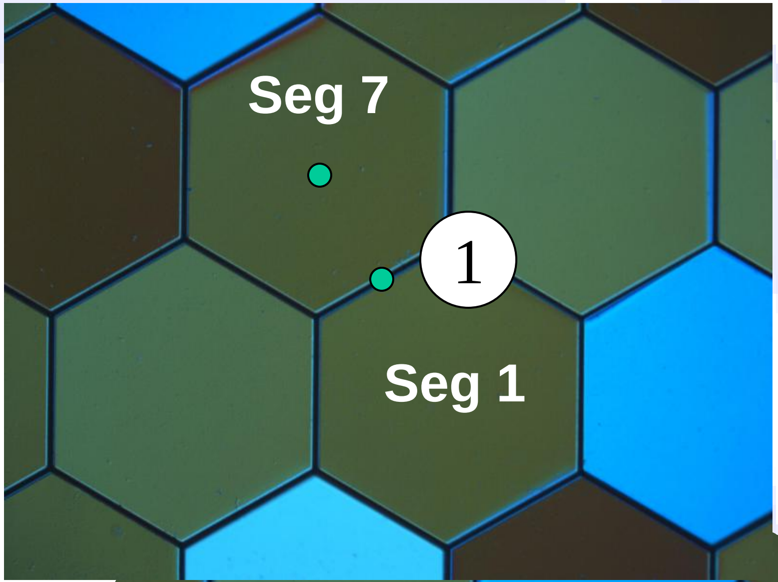
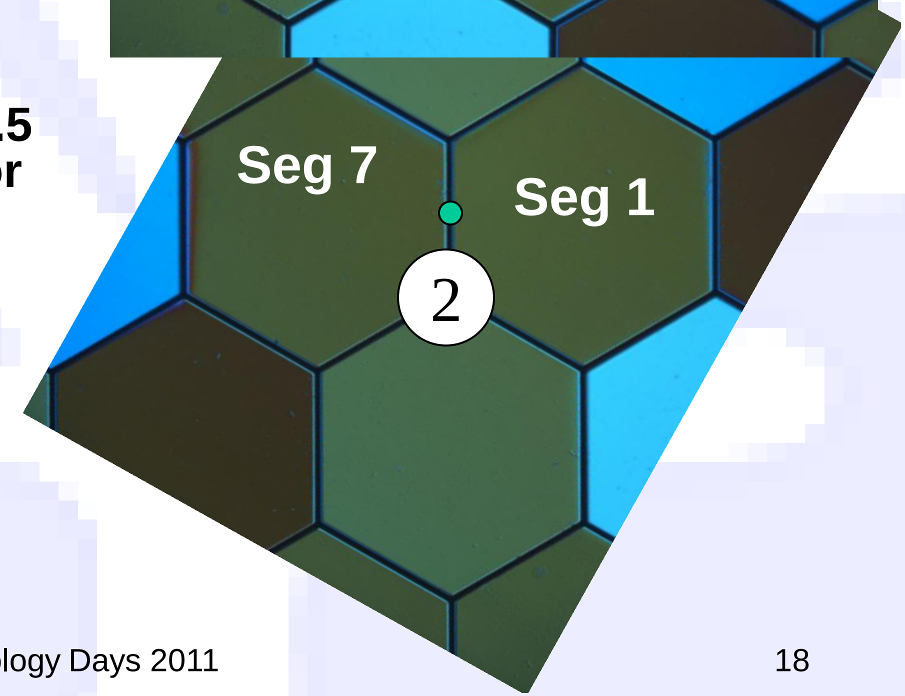
532 nm Laser Testing

- Standard packaging – no heatsinking
- 2W Gaussian beam, 25 μm waist
- 155 min CW onto DM segment and gaps
  - >200 kW/cm^2 in beam
  - 630 W/cm^2 onto segment
- Heating from 2W onto segment center
  - 14.6 °C from ambient
  - 8.7 °C above DM substrate
- 0.74W into the gap
  - Equivalent to average power of 18.5 W onto segment (96% fill factor for this DM)

1. Upper Image
   - 9.8 °C from ambient
   - 6.1 °C above DM substrate
2. Lower Image
   - 146.4 °C from ambient
   - 134.8 °C above DM substrate





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Thermal Model Projections (532nm tests)

- Assumptions
  - Limit deformations from heating to <λ/40 (13.3 nm *rms*)
  - Assume linear superposition
- Power handling of PTT111 DM
  - Existing packaging
    - 150 W/cm^2
    - 14 W onto PTT111 DM
  - Good heatsink case (Phase II)
    - 1200 W/cm^2
    - 110 W onto PTT111 DM

Phase II Goals

- Improve power handling capabilities: 1-2 kW/cm^2
  - Compensate for stress *and* CTE mismatches in the coatings
  - Increase fill factor to >98%
  - Packaging for lasers – heatsinking
- Improve mirror figure: <λ/40
- Speed improvements
  - Regain speed loses from using thicker 50 µm segments

Future Development Timeline

Testing Complete: CTE, Humidity

PTT489 Production Run

Fill Factor Improvements
Heatsinking

Phase I

Phase II – Year 1

Phase II – Year 2

July ‘11

Jan ‘13

Jan ‘14

CTE Compensation
Faster DM Design

Summary

- Lower unpowered segment position errors
  - < 200-300 nm *rms*
- Larger DM arrays
  - 10^3 actuators
- Improved laser power handling
  - 1-2 kW/cm^2
    - Changes in segment figure from laser heating $<\lambda/40$